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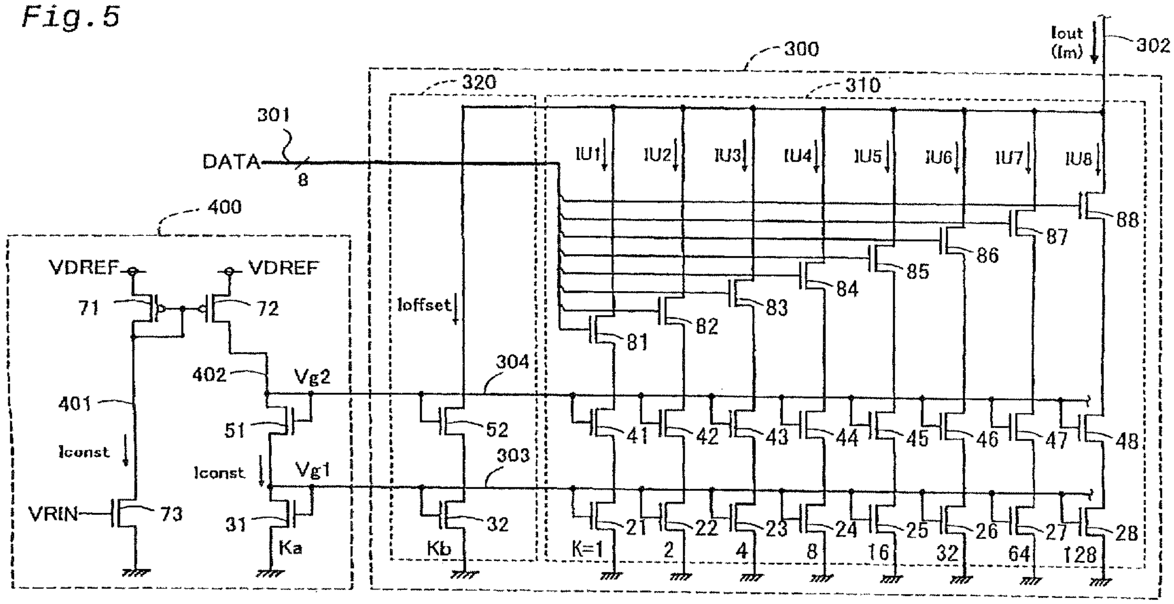
(54) Circuit for supplying the pixel in a luminescent display device with a prescribed current

(57) A data line drive circuit is equipped with a single line driver 300 and a gate voltage generation circuit 400. The single line driver 300 is constructed such that N groups (where N is an integer 2 or larger) of series connections of drive transistors 21 to 28 and switching transistors 81 to 88 are connected in parallel. The gate voltage generation circuit 400 includes two transistors 71 and 72 constituting a current mirror circuit, a drive transistor 73, and a constant voltage generation transistor 31. The range of an output current I_{out} can be controlled by changing any of the design values of the parameters including: relative values K_a and K_b of the gain coefficient for the transistors 31 and 32, the source voltage VDREF of the gate voltage generation circuit 400, and the gate signal VRIN of the drive transistor 73.

Fig.5



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Description

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] This invention relates to technology for generating a programming current supplied for setting the light emission level of a pixel circuit in a luminescent device.

Description of the Related Art

[0002] In recent years, electro-optical devices have been developed using organic electroluminescent devices. A backlight is unneeded for organic electroluminescent devices as they are self-luminescent, so it is expected that they will be used to achieve display devices with low power consumption, a wide viewing angle and a high contrast ratio. In the present specification, an "electro-optical device" refers to a device for converting electrical signals to light. The most common form of an electro-optical device is a display device for converting electrical signals representing images to light representing images.

[0003] In an active matrix driven electro-optical device using organic electroluminescent devices, a pixel circuit is provided to adjust the light emission level or luminescent scale of each organic electroluminescent device. The light emission level in each pixel circuit is set by supplying a voltage or current value to the pixel circuit corresponding to the light emission level. The method of setting a light emission level using voltage is called a voltage programming method, and that for setting a light emission level using a current value is called a current programming method. Herein, the term "programming" is used to mean "setting the light emission level". In the current programming method, the current used when programming a pixel circuit is called the "programming current". In a current programming type electro-optical device, a current generation circuit is used to generate a programming current having an accurate current value corresponding to the light emission level and supplying it to each pixel.

[0004] A programming current value corresponding to the light emission level, however, depends on the structure of the pixel circuit. The structure of pixel circuits often differs somewhat according to the design of the electro-optical device. Thus, there has been desired a current generation circuit whose range of output current values (programming current values) is easy to set according to the actual structure of the pixel circuit.

SUMMARY OF THE INVENTION

[0005] Accordingly, a first object of the present invention is to provide a technology with which the range of the programming current values can be set easily. A second object is to provide a current generation circuit with superior durability and productivity whose circuit structure is simple, and a driving method therefor, as well as electro-optical devices, semiconductor integrated circuit devices, and electronic devices using that current generation circuit.

[0006] In order to attain at least part of the above and other related objects of the present invention, there is provided an electro-optical device comprising: a pixel matrix in which pixels each including a luminescent element are arrayed in the form a matrix; a plurality of scan lines each connected to a pixel group arrayed in a row direction of the pixel matrix; a plurality of data lines each connected to a pixel group arrayed in a column direction of the pixel matrix; a scan line drive circuit, connected to the plurality of scan lines, for selecting one row in the pixel matrix; and a data line drive circuit for generating a data signal having a current value corresponding to a level of light to be emitted by the luminescent element, and outputting the data signal to at least one of the plurality of data lines. The data line drive circuit comprises: a current-addition type current generation circuit having a structure where N series connections of a first drive transistor for generating a prescribed current and a first switching transistor whose on/off switching is controlled in response to a control signal supplied by an external circuit are connected mutually in parallel, where N is an integer of 2 or greater; and a control-electrode signal generation circuit for generating a control-electrode signal having a prescribed signal level and supplying the control-electrode signal commonly to control electrodes of N number of first drive transistors.

[0007] The present invention is also directed to a current generation circuit comprising: constant current generation means; a signal input line; an output terminal; and current output means for outputting to the output terminal an output current generated based on a reference current supplied from the constant current generation means and on a signal supplied to the signal input line.

[0008] These and other objects, features, aspects, and advantages of the present invention will become more apparent from the following detailed description of the preferred embodiments with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009]

Fig. 1 is a block diagram showing the circuit structure of the photoelectric device 100 as one embodiment of the present invention.

Fig. 2 is a block diagram showing the internal structure of the display panel section 101 and the data line drive circuit 102.

Fig. 3 is a schematic diagram showing the internal

structure of the pixel circuit 200.

Figs. 4 (a) -4 (d) are timing charts showing the operation of the pixel circuit 200.

Fig. 5 is a schematic diagram showing the internal structure of the single line driver 300 and the gate voltage generation circuit 400.

Figs. 6 (a) and 6 (b) are explanatory diagrams showing an example of the relationships between the output current I_{out} from the data line drive circuit 102 and light emission level values.

Fig. 7 is a graph showing one example of the relationship between the output current I_{out} and the light emission level.

Fig. 8 is a block diagram showing the internal structure of the display panel section 101a and the data line drive circuit 102a in the second embodiment.

Fig. 9 is a perspective view showing the structure of a personal computer as one example of an electronic device to which the display device according to the present invention was applied.

Fig. 10 is a perspective view showing the structure of a portable telephone as one example of an electronic device to which the display device of the present invention was applied.

Fig. 11 is a perspective view showing the structure of the back side of a digital still camera as one example of an electronic device to which the display device of the present invention was applied.

DESCRIPTION OF THE PREFERRED EMBODIMENT

[0010] Embodiments of the present invention will be described below in the following sequence:

A. The overall structure of the device;
B. First embodiment;
C. Second embodiment;
D. Embodiments applied to electronic devices; and
E. Modified embodiments

A. The overall structure of the device:

[0011] Fig. 1 is a block diagram showing a circuit structure of an electro-optical device 100 as one embodiment of the present invention. The electro-optical device 100 is equipped with a display panel section 101 (referred to as a "pixel section") where the luminescent elements are disposed in the form of a matrix, a data line drive circuit 102 for driving the data lines in the display panel section 101, a scan line drive circuit 103 (also referred to as a "gate driver") for driving the scan lines (also referred to as "gate lines") in the display panel section 101, a memory 104 for storing display data provided by the computer 110, an oscillation circuit 106 for providing reference operation signals to other constituent elements, a power source circuit 107, and a control circuit 105 for controlling each constituent element in the electro-optical device 100.

[0012] The constituent elements 101 to 107 in the electro-optical device 100 may be constructed of independent parts thereof (for example, a semiconductor integrated circuit device of one chip), or a part or the entirety of the constituent elements 101 to 107 may be constructed as one piece. For example, the data line drive circuit 102 and the scan line drive circuit 103 may be constructed as one piece on the display panel section 101. Also, part of or the entirety of the constituent elements 102 to 106 may be constructed with a programmable IC chip whose function is implemented as software by a program written to the IC chip.

[0013] Fig. 2 shows the internal structure of the display panel section 101 and the data line drive circuit 102. The display panel section 101 is provided with a plurality of pixel circuits 200 arrayed in the form of a matrix, and each pixel circuit 200 includes an organic electroluminescent device 220. A plurality of data lines X_m (where m is from 1 to M) extending in the horizontal direction and a plurality of scan lines Y_n (where n is from 1 to N) extending in the vertical direction are each connected to the matrix of the pixel circuits 200. The data lines are also referred to as "source lines" and the scan lines are also referred to as "gate lines". In the present specification, the pixel circuits 200 are also referred to as "unit circuits" and "pixels". The transistors in the pixel circuits 200 are ordinarily constructed with a TFT.

[0014] The scan line drive circuit 103 selectively drives one of the plurality of scan lines Y_n, thereby selecting a group of pixel circuits in one row. The data line drive circuit 102 is provided with a plurality of single line drivers 300 for driving the data lines X_m respectively as well as with a gate voltage generation circuit 400. The gate voltage generation circuit 400 supplies the single line drivers 300 with a gate control signal having a prescribed voltage value. The internal structures of the gate voltage generation circuit 400 and the single line drivers 300 will be described later.

[0015] The single line drivers 300 provide data signals to the pixel circuits 200 through the data lines X_m. When the internal states (described below) of the pixel circuits 200 are set according to the data signals, the value of the current flowing at the organic electroluminescent devices 220 is accordingly controlled, resulting in the control of the luminescent stage of the organic electroluminescent device 220.

[0016] A control circuit 105 (Fig. 1) converts display data (pixel data) for representing the display state of the display panel section 101 to matrix data for representing the light emission level of each organic electrolumines-

cent device 220. The matrix data contains scan line drive signals for successively selecting a group of pixel circuits in one row and data line drive signals for indicating the level of the data line signal provided to the organic electroluminescent devices 220 in the selected group of pixel circuits. The scan line drive signal and data line drive signal are supplied to the scan line drive circuit 103 and the data line drive circuit 102, respectively. The control circuit 105 also controls the timing used for driving the scan lines and data lines.

[0017] Fig. 3 is a schematic diagram showing the internal structure of the pixel circuit 200. The pixel circuits 200 are disposed at the intersection of the m-th data line X_m and the n-th scan line Y_n. The scan lines Y_n contain two sub-scan lines V1 and V2.

[0018] The pixel circuit 200 is a current programming circuit for regulating the light emission level of the organic electroluminescent device 220 in response to the value of the current flowing in the data line X_m. In greater detail, the pixel circuit 200 has four transistors 211 to 214 and a storage capacitor 230 (referred to also as a "storage condenser" and a "memory capacitor") in addition to an organic electroluminescent device 220. The storage capacitor 230 holds an electrical charge in response to the data signal supplied through the data line X_m, and thereby regulates the light emission level of the organic electroluminescent device 220. In other words, the storage capacitor 230 holds a voltage in response to the current flowing in the data line X_m. The first to third transistors 211 to 213 are n-channel FETs; the fourth transistor 214 is a p-channel FET. The organic electroluminescent device 220 is a current injection (current driven) type luminescent element similar to a photodiode, and is represented here with a diode symbol.

[0019] The source of the first transistor 211 is connected to the drain of the second transistor 212, the drain of the third transistor 213 and the drain of the fourth transistor 214. The drain of the first transistor 211 is connected to the gate of the fourth transistor 214. The storage capacitor 230 is connected between the gate and the source of the fourth transistor 214. Also, the source of the fourth transistor 214 is connected to a power supply voltage Vdd.

[0020] The source of the second transistor 212 is connected to a single line driver 300 (Fig. 2) through a data line X_m. The organic electroluminescent device 220 is connected between the source of the third transistor 213 and the ground voltage.

[0021] The gates of the first and second transistors 211 and 212 are commonly connected to the first sub-scan line V1. Also, the gate of the third transistor 213 is connected to the second sub-scan line V2.

[0022] The first and second transistors 211 and 212 are switching transistors used when accumulating a charge in the storage capacitor 230. The third transistor 213 is a switching transistor held in an ON state during the luminescent interval of the organic electroluminescent device 220. The fourth transistor 214 is a drive transistor for controlling the value of the current flowing in the organic electroluminescent device 220. The value of the current in the fourth transistor 214 is controlled by the amount of charge (amount of accumulated charge) held in the storage capacitor 230.

[0023] Figs. 4 (a) -4(d) are timing charts indicating the operation of the pixel circuit 200. In the figure, the value of the voltage in the first sub-scan line V1 (hereinafter, referred to as the "first gate signal V1"), the value of the voltage in the second sub-scan line V2 (hereinafter, referred to as the "second gate signal V2"), the value of the current I_{out} in the data line X_m (hereinafter, referred to as the "data signal I_{out}"), and the value of the current IEL flowing in the organic electroluminescent device 220 are shown.

[0024] The driving period Tc is separated into a programming period T_{pr} and a light emission period T_{el}. The "driving period Tc" means the period during which the light emission levels of all the organic electroluminescent devices 220 in the display panel section 101 are updated one at a time and is equivalent to a so-called frame cycle. Updating of the light emission levels is carried out by groups of pixel circuits in a row wherein the light emission levels of N column pixel circuit group are successively updated during a driving period Tc. For example, when light emission levels of all the pixel circuits are being updated at 30 Hz, the driving period Tc is approximately 33 ms.

[0025] During the programming period T_{pr}, the light emission level of the organic electroluminescent devices 220 is set in the pixel circuit 200. In the present specification, the setting of light emission level to a pixel circuit 200 is referred to as "programming". For example, when the driving period Tc is approximately 33 ms, and the total number N of the scan lines Y_n is 480, the programming period T_{pr} is approximately 69 µs (33 ms/480) or less.

[0026] In the programming period T_{pr}, first, the second gate signal V2 is set to the L level, and the third transistor 213 is kept in an OFF state. Next, the first gate signal V1 is set to the H level and the first and second transistors 211 and 212 are switched to an ON state while the value of the current I_m flows on the data line X_m corresponding to the light emission level At this time, the single line drive 300 (Fig. 2) of the data line X_m functions as a constant current source in which the value of the current I_m flows constant corresponding to the light emission level. As indicated in Fig. 4 (c), the value of the current I_m is set according to the light emission level of the organic electroluminescent device 220 within a prescribed current range RI.

[0027] An electric charge corresponding to the value of the current I_m flowing through the fourth transistor 214 (drive transistor) is held in the storage capacitor 230. The voltage stored in the storage capacitor 230 is therefore applied between the source and gate of the fourth transistor 214. In the present specification, the value of the current I_m of the data signal used in programming is

referred to as the "programming current I_m".

[0028] When the programming is complete, the scan line drive circuit 103 sets the first gate signal V1 to the L level to turn the first and second transistors 211 and 212 to an OFF state. The data line drive circuit 102 stops the data signal I_{out}.

[0029] During the light emission period T_{el}, the second gate signal V2 is set to the H level and the third transistor 213 is switched to an ON state while the first gate signal V1 is maintained at the L level with the first and second transistors 211 and 212 held in an OFF state. A voltage corresponding to the programming current I_m is stored in the storage capacitor 230 beforehand, so a current that is about the same as the programming current I_m flows in the fourth transistor 214. Thus, a current nearly equal to the programming current I_m also flows in the organic electroluminescent device 220 which emits light at a level corresponding to the value of the current I_m. The type of pixel circuit 200 where the voltage in the storage capacitor 230 is written in this manner by the value of the current I_m is referred to as a "current programmable circuit".

B. First embodiment

[0030] Fig. 5 is a schematic diagram showing the internal structure of the single line driver 300 and the gate voltage generation circuit 400. The single line driver 300 is provided with an 8-bit D/A converter section 310 and an offset current generation circuit 320.

[0031] The D/A converter section 310 has eight current lines IU1 to IU8 connected in parallel. The first current line IU1 has a switching transistor 81, a resistance transistor 41 functioning as a type of resistor element, and a drive transistor 21 functioning as a constant current source in which a prescribed current flows, all connected in series between a data line 302 and a ground potential. The other current lines IU2 to IU8 have similar structures. The three types of transistors 81 to 88, 41 to 48 and 21 to 28 are all n-channel FETs in the example in Fig. 5. The gates of the eight drive transistors 21 to 28 are connected commonly to a first common gate line 303. Also, the gates of the eight resistance transistors 41 to 48 are connected commonly to a second common gate line 304. Each bit of the 8-bit data DATA provided by the control circuit 105 (Fig. 1) through a signal input line 301 is inputted to the gates of the eight switching transistors 81 to 88 respectively.

[0032] The ratio K of the gain coefficient β for the eight drive transistors 21 to 28 is set to 1:2:4:8:16:32:64:128. In other words, the relative value K of the gain coefficient β for the nth (where n is 1 to N) drive transistor is set to 2^{n-1}. The gain coefficient β is defined as $\beta = K\beta_o = (\mu C_o W/L)$ as is well known. K represents the relative value, β_o a prescribed constant, μ the carrier mobility, C_o the gate capacity, W the channel width, and L the channel length. The drive transistor number N is an integer of 2 or greater. The drive transistor number N is unrelated to the scan line Y_n number.

[0033] The eight drive transistors 21 to 28 function as constant current sources. The current drive capability of the transistors is proportional to the gain coefficient β, so the ratio of the current drive capability of the eight drive transistors 21 to 28 is 1:2:4:8:16:32:64:128. In other words, the relative value K of the gain coefficient for the drive transistors 21 to 28 is set to a value corresponding to the weight of each bit of the multi-level data DATA.

[0034] The current drive capability of the resistance transistors 41 to 48 is ordinarily set to a value at or above the current drive capability of the corresponding drive transistors 21 to 28. Thus, the current drive capability of the current lines IU1 to IU8 is determined by the drive transistors 21 to 28. The resistance transistors 41 to 48 acts as a noise filter for eliminating noise from the current value.

[0035] The offset current generation circuit 320 has a structure where a resistance transistor 52 and a drive transistor 32 are connected in series between the data line 302 and the ground potential. The gate of the drive transistor 32 is connected to the first common gate line 303, and the gate of the resistance transistor 52 is connected to the second common gate line 304. The relative value of the gain coefficient β for the drive transistor 32 is K_b. The offset current generation circuit 320 is not provided with a switching transistor between the drive transistor 32 and the data line 302, and in this way differs from the current lines in the D/A converter section 310.

[0036] The current line I_{offset} of the offset current generation circuit 320 is connected in parallel to the eight current lines IU1 to IU8 of the D/A converter section 310. Thus, the total current flowing in the nine current lines I_{offset} and IU1 to IU8 is outputted to the data line 302 as a programming current. More specifically, the single line driver 310 is a current-adding type current generation circuit. The reference symbols I_{offset} and IU1 to IU8 are hereinafter used to represent both the current lines and the currents flowing therein.

[0037] The gate voltage generation circuit 400 contains a current mirror circuit section comprising two transistors 71 and 72. The gates of the two transistors 71 and 72 are connected to each other as well as to the drain of the first transistor 71. One terminal (the source) of each of the transistors 71 and 72 is connected to a power supply voltage VDREF for the gate voltage generation circuit 400. A drive transistor 73 is connected in series on a first wire 401 between the other terminal (the drain) of the first transistor 71 and the ground potential. A control signal VRIN having a prescribed voltage level is inputted from the control circuit 105 to the gate of the drive transistor 73. A resistance transistor 51 and a constant voltage generation transistor 31 (also referred to as a "control electrode signal generation transistor") are connected in series on a second wire 402 between the other terminal (the drain) of the second transistor 72 and the ground potential. The relative value of the gain co-

efficient β for the constant voltage generation transistor 31 is K_a.

[0038] The gate and the drain of the constant voltage generation transistor 31 are connected to each other as well as to the first common gate line 303 of the single line driver 300. Also, the gate and drain of the resistance transistor 51 are connected to each other as well as to the second common gate line 304 of the single line driver 300.

[0039] In the example in Fig. 5, the two transistors 71 and 72 constituting the current mirror circuit are composed of p-channel FETs, and the other transistors are composed of n-channel FETs.

[0040] When a control signal VRIN with a prescribed voltage level is inputted to the gate of the drive transistor 73 of the gate voltage generation circuit 400, a constant reference current I_{const} is generated in response to the voltage level of the control signal VRIN on the first wire 401. The two transistors 71 and 72 constitute a current mirror circuit, so the same reference current I_{const} flows on the second wire 402 as well. There is no need, however, for the currents flowing on the two wires 401 and 402 to be identical, and in general, the first and second transistors 71 and 72 may be constructed so that the current on the second wire 402 is proportional to the reference current I_{const} on the first wire 401.

[0041] The current I_{const} causes prescribed gate voltages V_{g1} and V_{g2} between the gate and drain of the two transistors 31 and 51 respectively on the second wire 402. The first gate voltage V_{g1} is applied commonly to the gates of the nine drive transistors 32, 21-28 in the single line driver 300 through the first common gate line 303. Also, the second gate voltage V_{g2} is applied commonly to the gates of the nine resistance transistors 52, 41-48 through the second common gate line 304.

[0042] The current drive capabilities of the current lines I_{offset}, IU1-IU8 are determined by the gain coefficients β of the respective drive transistors 32, 21-28 and the applied gate voltage. Thus, a current flowing whose value is proportional to the relative value K of the gain coefficient β of each drive transistor can be obtained in response to the gate voltage V_{g1} at each respective current line I_{offset}, IU1-IU8 of the single line driver 300. When an 8-bit data DATA is provided by the control circuit 105 through the signal input line 301, the on/off switching of the eight switching transistors 81 to 88 is controlled in response to the value of each bit of the multi-bit data DATA. As a result, a programming current I_m having a current value corresponding to the value of the multi-bit data DATA is outputted to the data line 302.

[0043] It should be noted that the single line driver 300 includes the offset current generation circuit 320, so the value of the multi-bit data DATA and the programming current I_m have an offset and their graphical relationship is not a proportional one passing through the origin. Providing this offset has the advantage that the degree of freedom in setting the range of the programming current values is increased, so the programming current values can be easily set to have a favorable range.

[0044] Figs. 6 (a) and 6 (b) show Examples 1 to 5 with the relationship of the output current I_{out} of the data line drive circuit 102 with the level of the multi-bit data DATA. The table of Fig. 6 (a) shows the reference Example 1 as well as Examples 2 to 5 in which the below four parameters have been changed respectively.

(1) VRIN: The voltage value of the gate signal for the drive transistor 73 in the gate voltage generation circuit 400.

(2) VDREF: The source voltage of the current mirror circuit in the gate voltage generation circuit 400.

(3) K_a: The relative value of the gain coefficient β for the constant voltage generation transistor 31 in the gate voltage generation circuit 400.

(4) K_b: The relative value of the gain coefficient β of the drive transistor 32 in the offset current generation circuit 320.

[0045] Fig. 6 (b) shows the relationships in Fig. 6 (a) in a graph. In Example 1, which is used as the "reference," each parameter is set to a prescribed reference value. In Example 2, only the voltage VRIN of the drive transistor 73 was set to a higher value than that of the reference Example 1. In Example 3, only the source voltage VDREF of the current mirror circuit is set to a higher value than that of the standard Example 2. In Example 4, only the relative value K_a of the gain coefficient β for the constant voltage generation transistor 31 is set to a higher value than that of the reference Example 1. In Example 5, only the relative value K_b of the gain coefficient β for the drive transistor 32 is set to a higher value than that of the reference Example 1.

[0046] As shown in the table and the graph, the value of the output current I_{out} varies according to each of the VRIN, VDREF, K_a and K_b parameters. Thus, the range of the current values used for controlling the light emission level can be changed by changing at least one of these parameters. The values of the VRIN, VDREF, K_a and K_b parameters are set by adjusting the design values of the circuit parts related respectively thereto. In the circuit structure shown in Fig. 5, all of the four parameters VRIN, VDREF, K_a and K_b affect the range of the output current I_{out}, so the degree of freedom when setting the range of the output current I_{out} is high, giving the advantage that it can be easily set to an arbitrary range.

[0047] It should be noted here that the output current I_{out} is proportional to the reference current I_{const} in the gate voltage generation circuit 400. Thus, the reference current I_{const} is determined in response to the range of the current values required by the output current I_{out} (in other words, the programming current I_m). At that time, there is the possibility that if the reference current I_{const} value is set close to one of the ends of the range of the current values required as output current I_{out}, a small variance or error in the reference current I_{const} may

cause a large variance or error in the output current I_{out} due to the performance of the circuit parts. Thus, in order to decrease the error in the output current I_{out}, it is favorable to set the value of the reference current I_{const} close to the midpoint between the minimum and maximum values of the current value range of the output current I_{out}. Here, "close to the midpoint between the minimum and maximum values" is meant to be a range of about -10% to about +10% of the average or center value of the minimum and maximum values.

[0048] Fig. 7 is a graph showing an example relationship between the output current I_{out} and the light emission level. In this example, the 256 levels from 0 to 255 is expressed by an output current I_{out} with a range from 0 to 5000 nA. In this case, t is favorable to set the value of the reference current I_{const} to around 2500 nA, which is the midpoint therefor.

[0049] The relative value K_n of the gain coefficient β for the constant voltage generation transistor 31 may be set to a value equivalent to the central value (128) of the light emission level range in order to set the value of the reference current I_{const} to the equivalent value of the output current I_{out} corresponding to the central value (128) of the light emission level range in the circuit in Fig. 5.

[0050] As explained above, the data line drive circuit 102 in the first embodiment has the advantage that the design value of one or more parameters may be arbitrarily changed to arbitrarily regulate the range of the output current I_{out} and the programming current I_m. There is another advantage that the circuit 102 has excellent durability and productivity because its structure is extremely simple.

C. Second Embodiment:

[0051] Fig. 8 shows the internal construction of a display panel section 101a and a data line drive circuit 102a in the second embodiment. In this display device, one single line driver 300 and a shift register 500 are provided in place of the plurality of single line drivers 300 in the structure in Fig. 2. A switching transistor 520 is provided on each data line of the display panel section 101a. One terminal of each switching transistor 520 is connected to the data lines X_m, and the other terminal is commonly connected to an output signal line 302 of the single line driver 300. A shift register 500 supplies an on/off control signal to the switching transistor 520 of each data line X_m whereby the data lines X_m are successively selected.

[0052] In this display device, pixel circuits 200 are successively updated in point succession. More specifically, only one pixel circuit 200 at the intersection of a gate line Y_n selected by a scan line drive circuit 103 and a data line X_m selected by the shift register 500 is updated with a single programming operatirin. For example, programming is successively carried out on M number of the pixel circuits 200 one at a time selected by the nth gate line Y_n, after which the M number of pixel circuits 200 on the next (n+1) th gate line are programmed one at a time. In contrast to this, the display device indicated in Fig. 8 and its operation differ from that of the first embodiment described above where a group of pixel circuits in one row are programmed at the same time (i.e., in line succession).

[0053] When programming is performed by the pixel circuits 200 in point succession as in the display device in Fig. 8, the same single line driver 300 and gate voltage generation circuit 400 are used as in the first embodiment described above in order to generate an output current I_{out} and programming current I_m having a desired current range.

D. Embodiments applied to electronic devices:

[0054] A display device using an organic electroluminescent device may be applied to a variety of electronic devices such as mobile personal computers, cellular phones and digital still cameras.

[0055] Fig. 9 is a perspective view of a mobile personal computer. A personal computer 1000 is equipped with a main body 1040 having a keyboard 1020, and a display unit 1060 using organic electroluminescent devices.

[0056] Fig. 10 is a perspective view of a cellular phone. A cellular phone 2000 is equipped with a plurality of operation keys 2020, an ear piece 2040, a mouthpiece 2060, and a display panel 2080 using organic electroluminescent devices.

[0057] Fig. 11 is a perspective view of a digital still camera 3000. Connections to external devices are indicated in a simplified fashion. While a conventional camera exposes film to the optical image of the object, the digital still camera 3000 generates an image signal through a photoelectric transfer by an image element such as a CCD (charge coupled device) of the optical image of the object. A display panel 3040 using organic electroluminescent devices is provided at the back of a case 3020 of the digital still camera 3000, and display is made based on image signals from the CCD. The display panel 3040 thus functions as a viewfinder to display the object. Also, a photo receiving unit 3060 including an optical lens and a CCD is provided on the observation side of the case 3020 (the back side in the figure) .

[0058] When the photographer verifies the object displayed in the display panel 3040 and presses a shutter button 3080, the image signal of the CCD at that time is forwarded and stored in memory in a circuit board 3100. This digital still camera 3000 is provided with a video signal output terminal 3120 and a data communication I/O terminal 3140 at the side of the case 3020. As indicated in the figure, a television monitor 4300 may be connected to this video signal output terminal 3120 and a personal computer 4400 may be connected to the I/O terminal 3140 for data transmission according to need. Further, a prescribed operation may be used to output image signals stored in memory in the circuit board 3100

to the television monitor 4300 or the personal computer 4400.

[0059] Examples of electronic devices other than the personal computer in Fig. 9, the portable telephone in Fig. 10, and the digital still camera 3000 in Fig. 11 includes television monitor, a view finder or monitoring direct view type video tape recorder, a car navigation device, a pager, an electronic notebook, a calculator, a word processor, a work station, a video telephone, a POS terminal, and devices with a touch panel. The display device described above using organic electroluminescent devices may be applied to the display section of such electronic devices.

E. Modified embodiments:

[0060]

Modification E1:

In the embodiment shown in Fig. 5, the resistance transistors 52, 41-48 are connected to the drive transistors 32, 21-28, but it is possible to replace the resistance transistors 52, 41-48 with other resistance elements or resistance adding means as well. Also, such resistance elements need not be necessarily be connected to all the drive transistors 31, 21-28, but may be provided according to need.

Modification E2:

Part of the circuit structure in Fig. 5 may be omitted. For example, the offset current generation circuit 320 may be omitted. If, however, the offset current generation circuit 320 is to be provided, the degree of freedom in setting the range of the programming current values increases, giving the advantage that setting a favorable range of programming current values is easy to do.

Modification E3:

In the embodiments described above, a part or all of the transistors may be replaced with bipolar transistors, thin film diodes or other types of switching elements. The gate electrodes of FETs and the base electrodes of bipolar transistors correspond to the "control electrodes" in the present invention.

Modification E4:

In the embodiments described above, the display panel section 101 has one pixel circuit matrix set, but it may have a plurality of sets of pixel circuit matrices as well. For example, when constructing a large panel, the display panel section 101 may be separated into a plurality of regions, and one pixel circuit matrix set may be provided for each region. Also, three pixel circuit matrix sets corresponding to the three RGB colors may be provided in one display panel section 101. When there is a plurality of pixel circuit matrices the embodiments described above may be applied for each matrix.

Modification E5:

The pixel circuit used in the embodiments described above is separated into a programming period T_{pr} and a light emission period T_{el}, but it is also possible to use a pixel circuit where the programming period T_{pr} is present within a portion of the light emission period T_{el}. For such a pixel circuit, the programming is carried out and the light emission level is set in the initial stage of the light emission period T_{el}, after which the light emission continues with the set level. The data line drive circuits described above may be applied to a device using such a pixel circuit as well.

Modification E6:

In the embodiments described above, example display devices using organic electroluminescent devices are described, but the invention may be applied to display devices and electronic devices using electroluminescent devices other than organic electroluminescent devices as well. For example, it is possible to apply electroluminescent devices where the light emission level can be adjusted in response to the drive current (such as LEDs and FEDs (field emission displays)) as well as other types of electroluminescent devices.

Modification E7:

The present invention is not limited to circuits and devices which include pixel circuits and which are driven using an active driving method and, and the present invention is also applicable to circuits and devices which do not include pixel circuits and which are driven with a passive driving method.

[0061] Although the present invention has been described and illustrated in detail, it is clearly understood that the same is by way of illustration and example only and is not to be taken by way of limitation, the spirit and scope of the present invention being limited only by the terms of the appended claims.

Claims

1. An electro-optical device comprising:

   a pixel matrix in which pixels each including a luminescent element are arrayed in the form a matrix;
   a plurality of scan lines each connected to a pixel group arrayed in a row direction of the pixel matrix;
   a plurality of data lines each connected to a pixel group arrayed in a column direction of the pixel matrix;

a scan line drive circuit, connected to the plurality of scan lines, for selecting one row in the pixel matrix; and

a data line drive circuit for generating a data signal having a current value corresponding to a level of light to be emitted by the luminescent element, and outputting the data signal to at least one of the plurality of data lines;

wherein the data line drive circuit comprises:

a current-addition type current generation circuit having a structure where N series connections of a first drive transistor for generating a prescribed current and a first switching transistor whose on/off switching is controlled in response to a control signal supplied by an external circuit are connected mutually in parallel, where N is an integer of 2 or greater; and

a control-electrode signal generation circuit for generating a control-electrode signal having a prescribed signal level and supplying the control-electrode signal commonly to control electrodes of N number of first drive transistors.

2. An electro-optical device of Claim 1, wherein the control-electrode signal generation circuit includes:

a control-electrode signal generation transistor having a first control electrode for generating the control-electrode signal at the first control electrode; and

a constant current circuit for generating a constant current flowing in the control-electrode signal generation transistor,

and wherein the first control electrode of the control-electrode signal generation transistor and the control electrodes of the N number of first drive transistors of the current generation circuit are mutually connected.

3. An electro-optical device according to Claim 2, wherein the constant current circuit includes:

a current mirror circuit, having two transistors connected respectively to a first and a second wire, for generating a current on the second wire proportional to a current on the first wire; and

a second drive transistor, connected to the first wire, for generating a prescribed current on the first wire in response to a control signal provided by an external circuit,

and wherein the control-electrode signal generation transistor is connected to the second wire.

4. An electro-optical device according to Claim 2 or 3, wherein the current generation circuit further includes:

a third drive transistor, coupled in parallel with the N series connections of the first drive transistor and the first switching transistor, for generating an offset current,

and wherein a control electrode of the third drive transistor is connected to the first control electrode of the control-electrode signal generation transistor without a switching transistor being provided between the third drive transistor and the data line.

5. An electro-optical device according to any of Claims 1 to 4,
wherein each series connection between the first drive transistor and the first switching transistor includes a resistor element.

6. An electro-optical device according to Claim 5, wherein the resistor element is a transistor.

7. An electro-optical device according to any of Claims 1 to 6,
wherein the N number of first drive transistors are constructed such that a relative values of a gain coefficient for a nth transistor in the N number of first drive transistors is 2^{n-1}, where n is an integer between 1 and N.

8. An electro-optical device according to any of Claims 1 to 7,
wherein the pixel matrix is driven using an active matrix driving technique.

9. An electro-optical device according to any of Claims 1 to 7,
wherein the pixel matrix is driven using a passive matrix driving technique.

10. A data line drive circuit for generating a data signal having a current value corresponding to a light emission level of a luminescent element, and outputting the data signal on a data line connected to an pixel including the luminescent element, the data line drive circuit comprising:

a current-addition type current generation circuit having a structure where N series connections of a first drive transistor for generating a prescribed current and a first switching transistor whose on/off switching is controlled in response to a control signal supplied by an external circuit are connected mutually in parallel, where N is an integer of 2 or greater; and

a control-electrode signal generation circuit for

generating a control-electrode signal having a prescribed signal level and supplying the control-electrode signal commonly to control electrodes of N number of first drive transistors.

11. A data line drive circuit according to Claim 10, wherein the control-electrode signal generation circuit includes:

a control-electrode signal generation transistor having a first control electrode for generating the control-electrode signal at the first control electrode; and
a constant current circuit for generating a constant current flowing in the control-electrode signal generation transistor,
and wherein the first control electrode of the control-electrode signal generation transistor and the control electrodes of the N number of first drive transistors of the current generation circuit are mutually connected.

12. A data line drive circuit according to Claim 10, wherein the constant current circuit includes:

a current mirror circuit, having two transistors connected respectively to a first and a second wire, for generating a current on the second wire proportional to a current on the first wire; and
a second drive transistor, connected to the first wire, for generating a prescribed current on the first wire in response to a control signal provided by an external circuit,
and wherein the control-electrode signal generation transistor is connected to the second wire.

13. A data line drive circuit according to Claim 11 or 12, wherein the current generation circuit further includes:

a third drive transistor, coupled in parallel with the N series connections of the first drive transistor and the first switching transistor, for generating an offset current,
and wherein a control electrode of the third drive transistor is connected to the first control electrode of the control-electrode signal generation transistor without a switching transistor being provided between the third drive transistor and the data line.

14. A data line drive circuit according to any of Claims 10 to 13,
wherein each series connection between the first drive transistor and the first switching transistor includes a resistor element.

15. A data line drive circuit according to Claim 14, wherein the resistor element is a transistor.

16. A data line drive circuit according to any of Claims 10 to 15,
wherein the N number of first drive transistors are constructed such that a relative values of a gain coefficient for a nth transistor in the N number of first drive transistors is 2^{n-1}, where n is an integer between 1 and N.

17. A data line drive circuit according to any of Claims 10 to 16,
wherein the pixel matrix is driven using an active matrix driving technique.

18. A data line drive circuit according to any of Claims 10 to 16,
wherein the pixel matrix is driven using a passive matrix driving technique.

19. A current generation circuit comprising:

constant current generation means;
a signal input line;
an output terminal; and
current output means for outputting to the output terminal an output current generated based on a reference current supplied from the constant current generation means and on a signal supplied to the signal input line.

20. A current generation circuit according to Claim 19, wherein the constant current generation means includes a current mirror circuit.

21. A current generation circuit according to Claim 19 or Claim 20,
wherein the constant current generation means includes at least one reference voltage source.

22. A current generation circuit according to any of Claims 19 to 21
wherein the current output means includes a plurality of first transistors having different gain coefficients.

23. A current generation circuit according to Claim 22, wherein the current output means generates the output current by synthesizing current flowing in one or more transistors selected from the plurality of first transistors by the signal to the signal input line.

24. A current generation circuit according to Claim 22 or 23,
wherein the constant current generation means includes a second transistor connected to a gate elec-

trode of the first transistor.

25. A current generation circuit according to Claim 24, wherein the second transistor has a function of converting the reference current to a gate voltage at the plurality of first transistors.

26. A current generation circuit according to any of Claims 22 to 25, further comprising first resistance adding means, disposed between the output terminal and the plurality of first transistors, with respect to at least one of the plurality of first transistors.

27. A current generation circuit according to Claim 26, wherein the first resistance adding means is a third transistor.

28. A current generation circuit according to Claim 27, wherein the constant current generation means includes a fourth transistor connected to a gate electrode of the third transistor.

29. A current generation circuit according to any of Claims 19 to 28,
wherein the current output means includes an offset current path for regulating a minimum value of the output current.

30. A current generation circuit according to Claim 24, wherein the current output means includes an offset current path for regulating a minimum value of the output current, and
the offset current path has a fifth transistor whose gate electrode is connected to the second transistor.

31. A current generation circuit according to Claim 30, further comprising second resistance adding means disposed between the output terminal and the fifth transistor.

32. A current generation circuit according to Claim 31, wherein the second resistance adding means is a sixth transistor.

33. A drive method of the current generation circuit according to any of Claims 19 to 32, wherein the reference current is set to a value close to a center value of minimum and maximum values of the output current.

34. A drive method of the current generation circuit according to any of Claims 30 to 32, wherein the output current is adjusted by variation of a gain coefficient of the fifth transistor.

35. An electro-optical device comprising:

a plurality of scan lines;
a plurality of data lines;
an electro-optical device disposed at each intersection of the scan lines and the data lines;
a scan line drive circuit for driving the scan lines; and
a data line drive circuit for driving the data lines, the data line drive circuit including any one of the current generation circuits according to any one of Claims 19 to 32, and means for inputting an output current from the current generation circuit to the data line.

36. An electro-optical device according to Claim 35, wherein the electro-optical element is a current-driven type device.

37. An electro-optical device according to Claim 36, wherein the current-driven type device is an organic electroluminescence device.

38. An electro-optical device according to any of Claims 35 to 37, further comprising:

a memory for storing data to be supplied to the electro-optical device; and
a control circuit for supplying the data read from the memory to the data line drive circuit and the scan line drive circuit as the signal; thereby controlling the scan line drive circuit and the data line drive circuit.

39. An electro-optical device according to any of Claims 35 to 38, further comprising an oscillation circuit for supplying a reference operation signal to a specific circuit constituting a driving system of the electro-optical device.

40. A semiconductor integrated circuit device comprising the current generation circuit according to any one of Claims 19 to 32.

41. An electronic device comprising the electro-optical device according to any one of Claims 35 to 38.

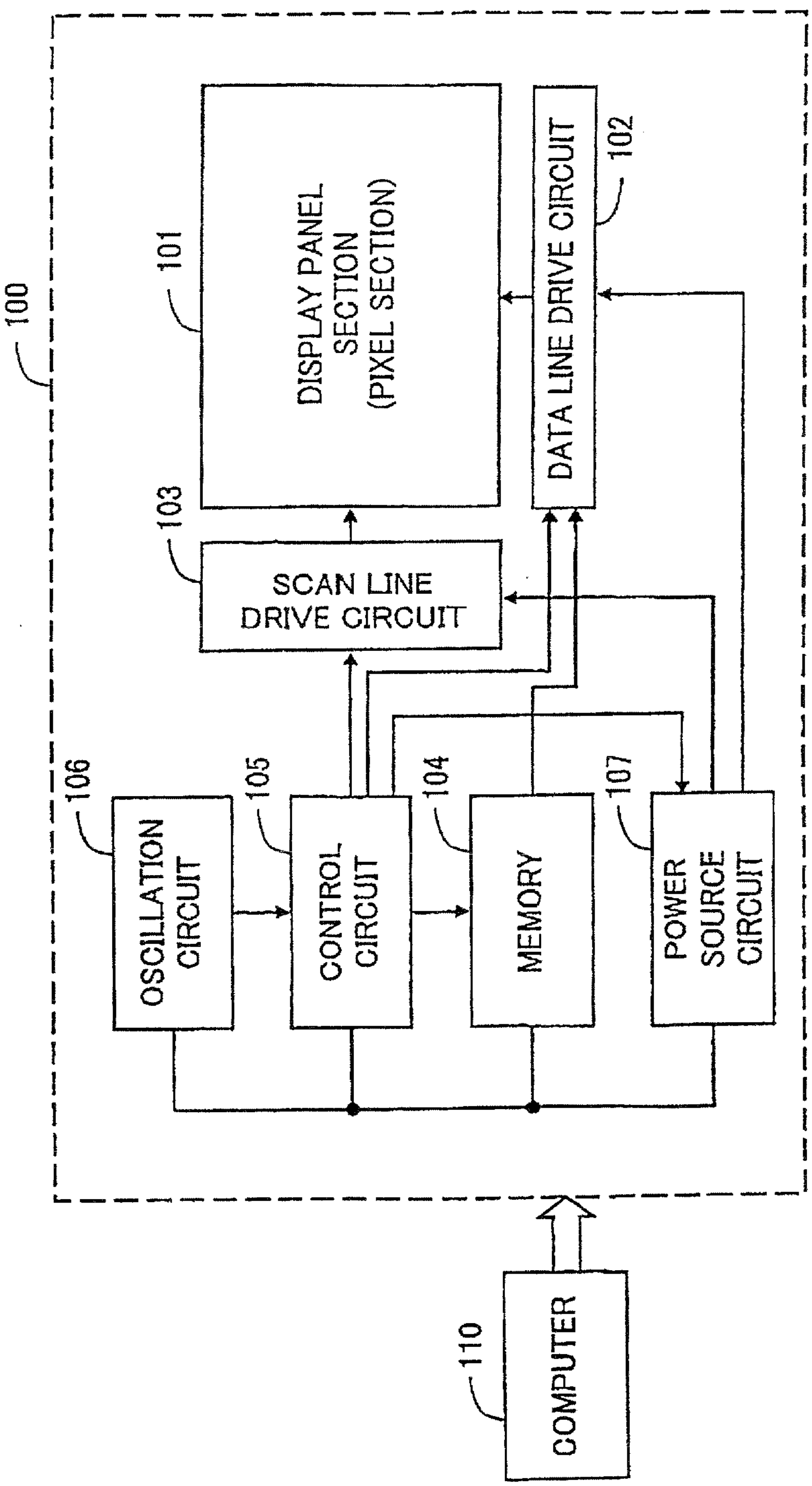

100
101
DISPLAY PANEL SECTION (PIXEL SECTION)
102
DATA LINE DRIVE CIRCUIT
103
SCAN LINE DRIVE CIRCUIT
106
OSCILLATION CIRCUIT
105
CONTROL CIRCUIT
104
MEMORY
107
POWER SOURCE CIRCUIT
110
COMPUTER

Fig.1

Fig.2

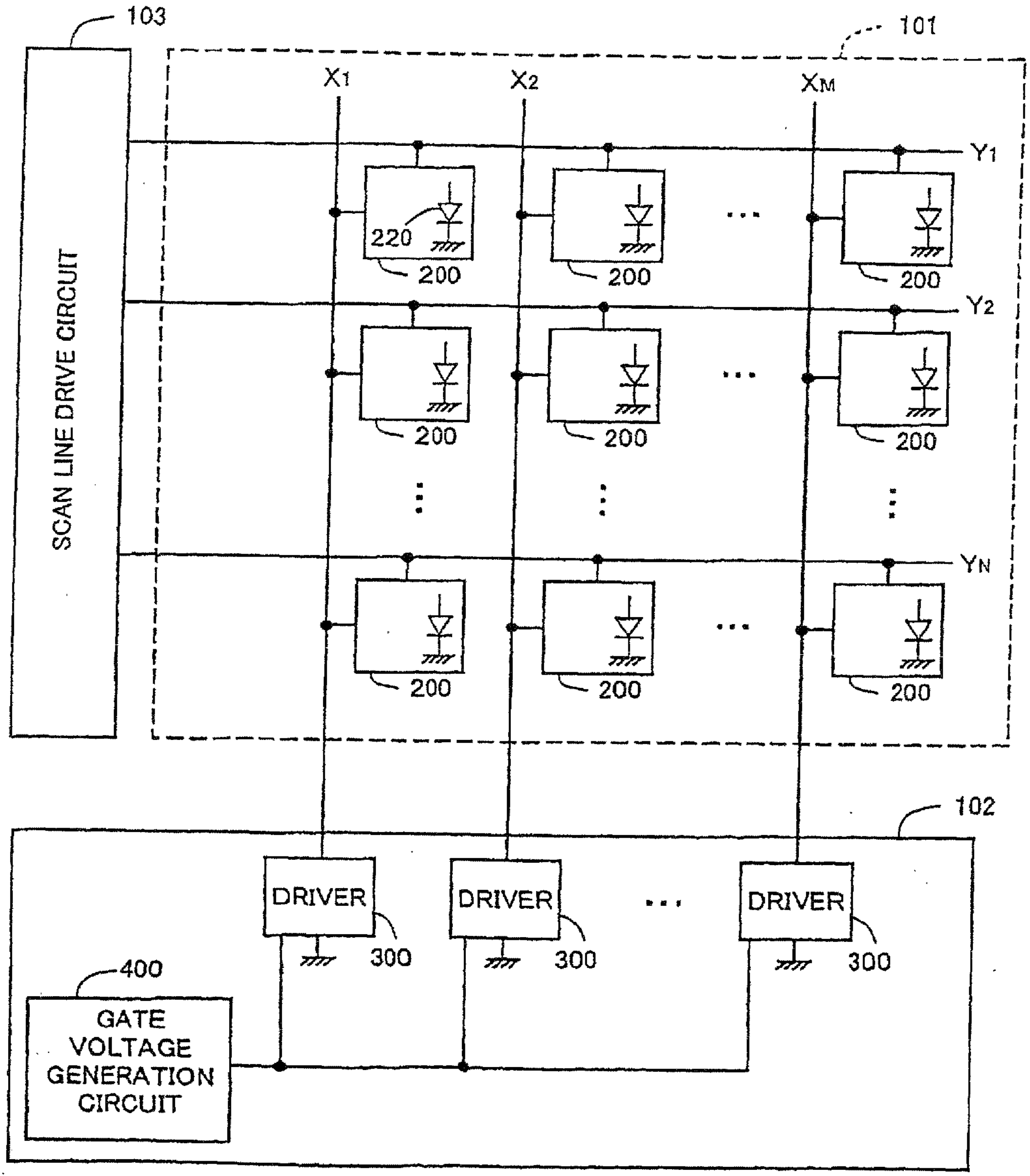
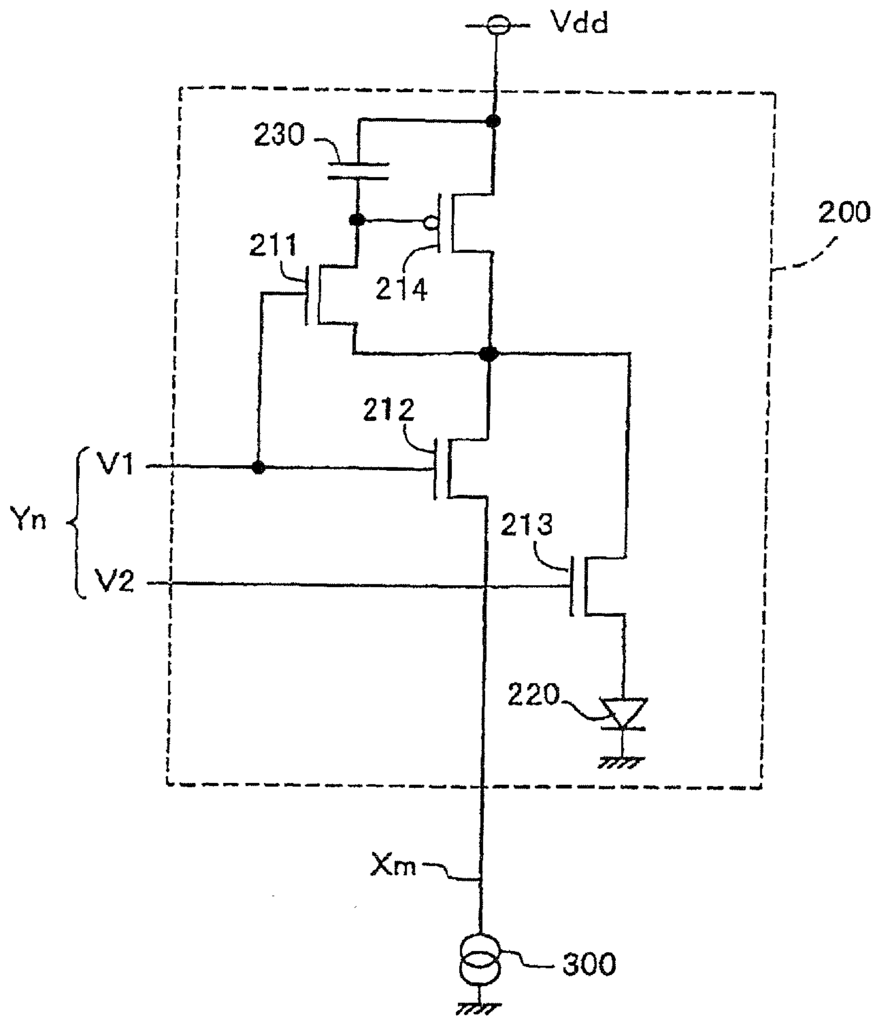

103
101
SCAN LINE DRIVE CIRCUIT
X1
X2
XM
Y1
Y2
YN
220
200
102
DRIVER
300
400
GATE VOLTAGE GENERATION CIRCUIT

Fig.3



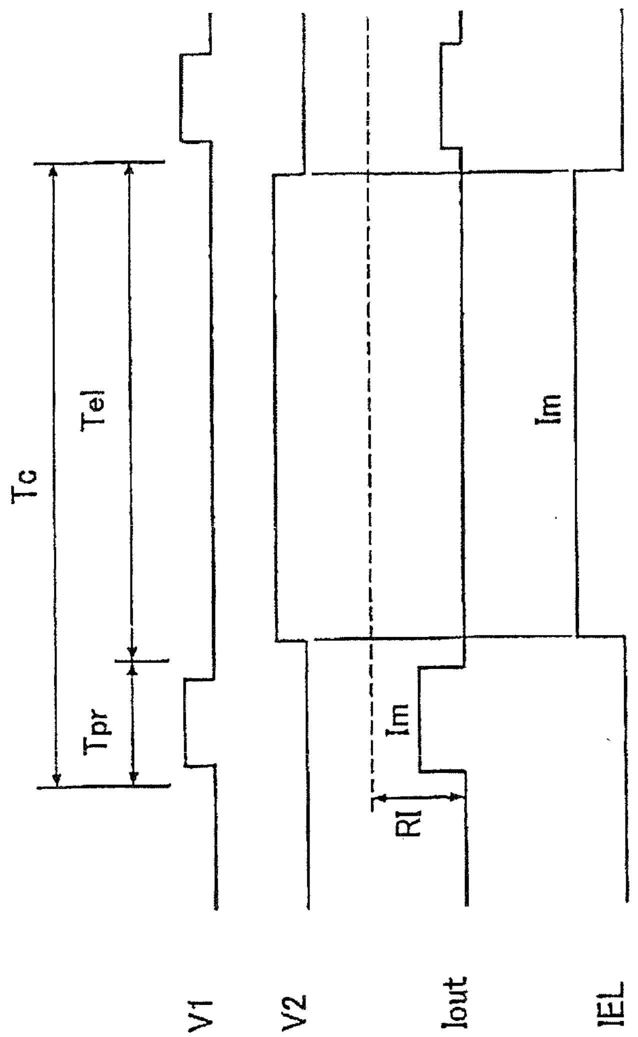


Fig.4(a)

Fig.4(b)

Fig.4(c)

Fig.4(d)

Fig.5

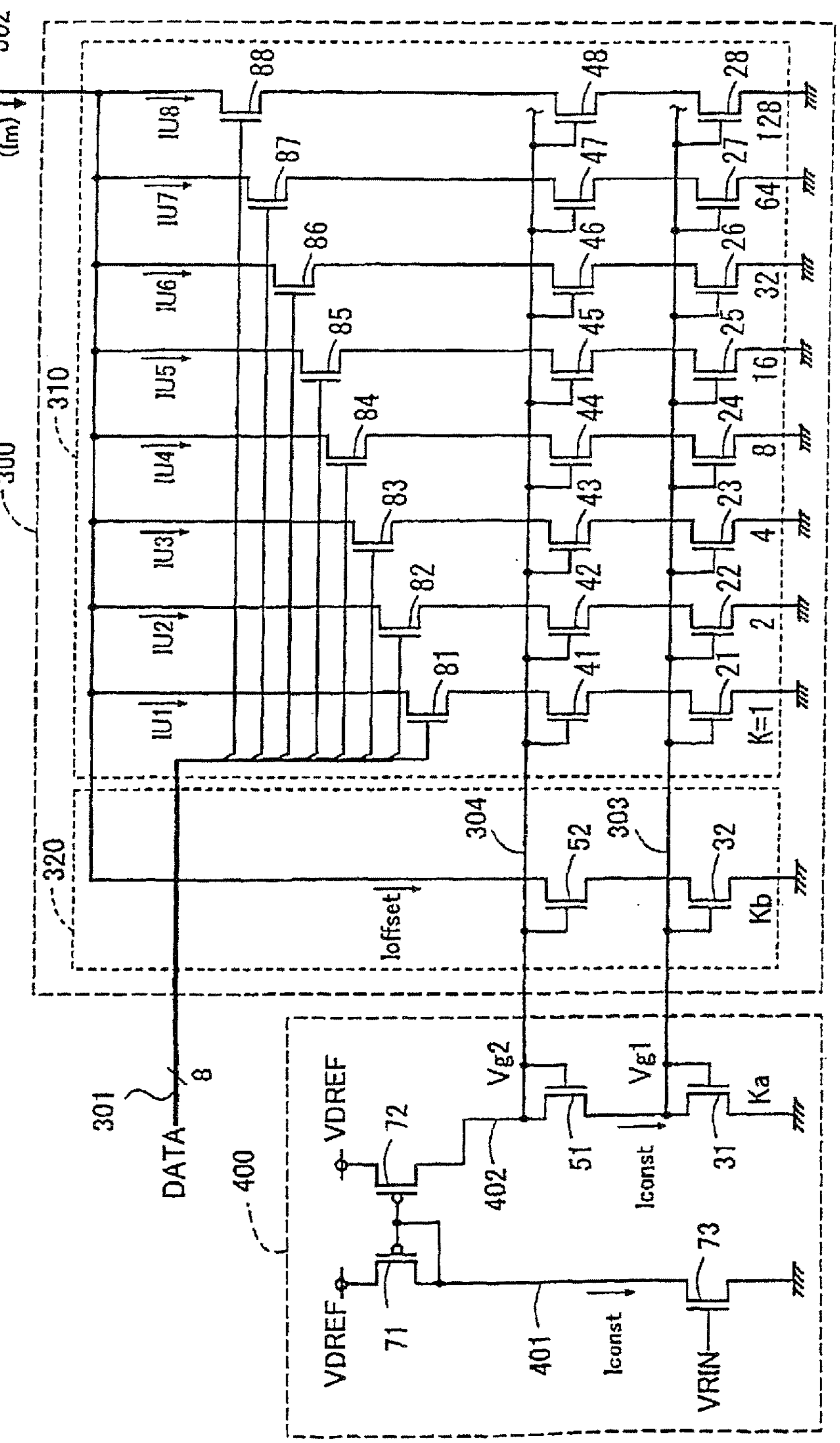

302
Iout
(Im)
300
310
320
IU1
IU2
IU3
IU4
IU5
IU6
IU7
IU8
81
82
83
84
85
86
87
88
41
42
43
44
45
46
47
48
21
22
23
24
25
26
27
28
K=1
2
4
8
16
32
64
128
304
303
52
32
Ioffset
Kb
301
DATA
8
400
VDREF
72
402
Vg2
51
Iconst
Vg1
31
Ka
71
401
73
VRIN

Fig.6(a)

<Example of Iout change due to parameter adjustment>

	Example 1	Example 2	Example 3	Example 4	Example 5
Level	Standard	VRIN large	VDREF large	Ka large	Kb large
1	520	1040	780	364	920
15	800	1600	1200	560	1200
31	1120	2240	1680	784	1520
63	1760	3520	2640	1232	2160
127	3040	6080	4560	2128	3440
255	5600	11200	8400	3920	6000
Graph	G1	G2	G3	G4	G5

(Ioffset =500)

Fig.6(b)

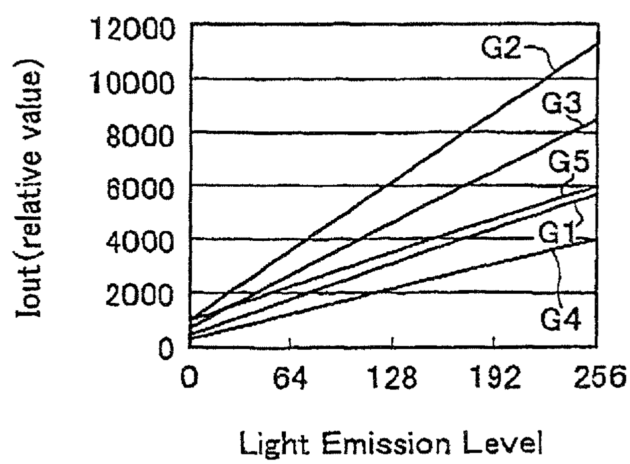


Fig. 7

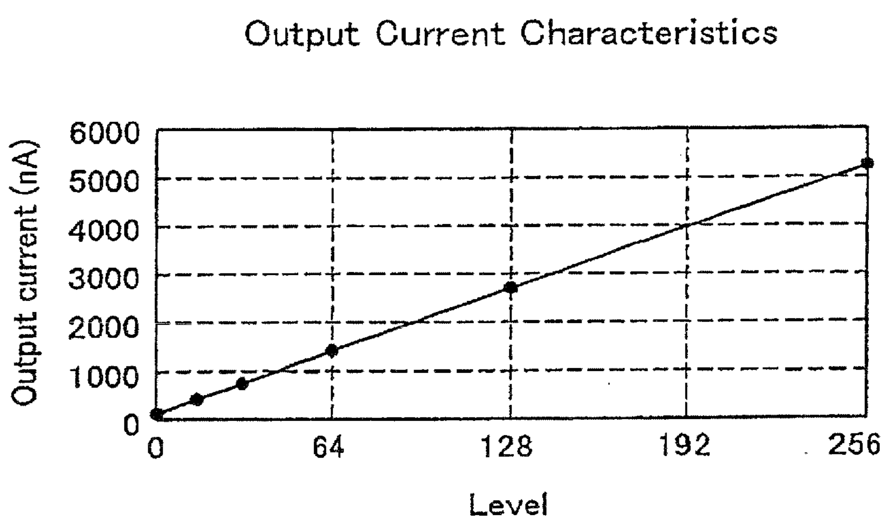

Output Current Characteristics
Output current (nA)
6000
5000
4000
3000
2000
1000
0
0
64
128
192
256
Level

Fig.8

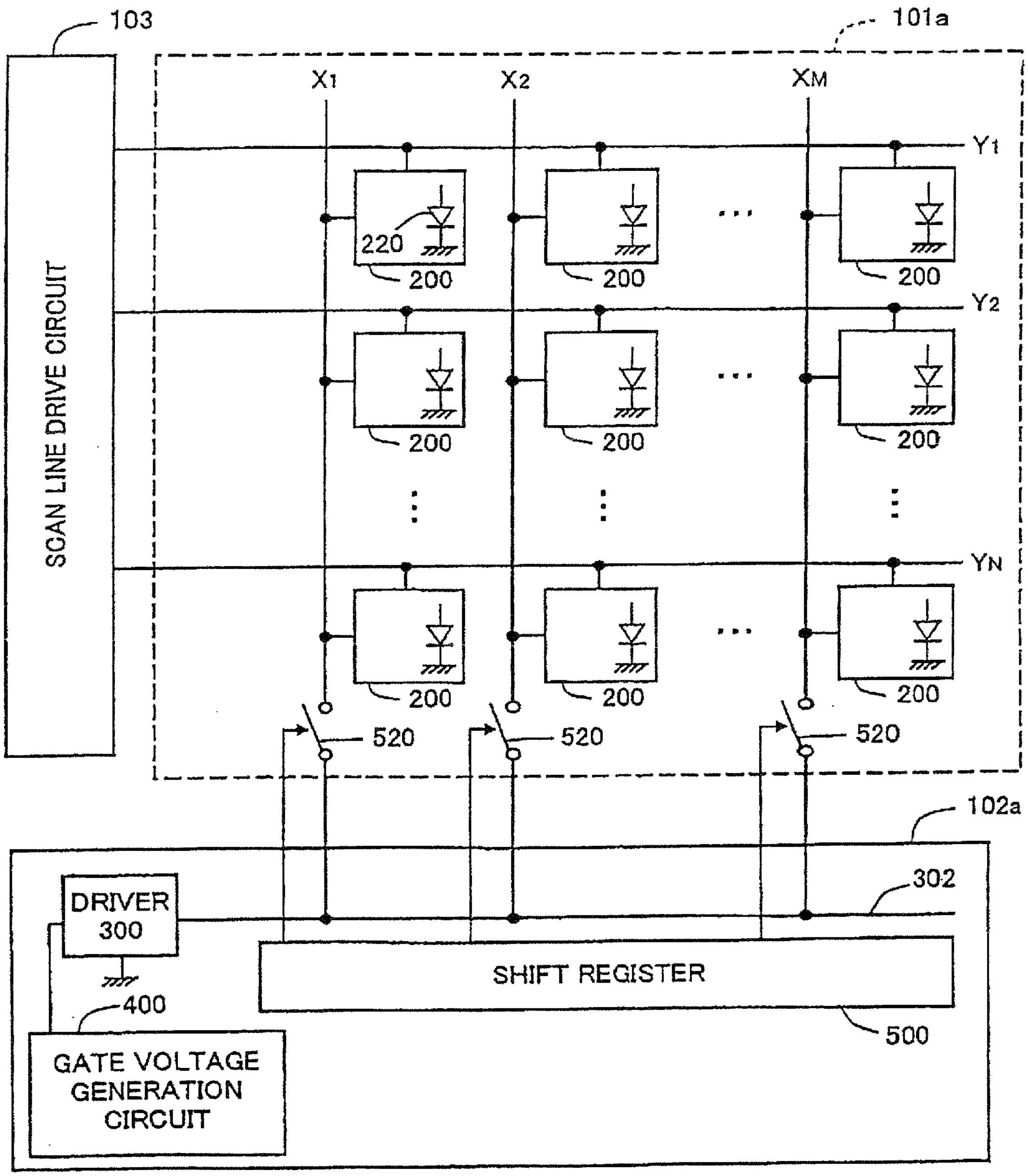

103
101a
SCAN LINE DRIVE CIRCUIT
X1
X2
XM
Y1
Y2
YN
220
200
520
102a
302
DRIVER
300
400
SHIFT REGISTER
500
GATE VOLTAGE
GENERATION
CIRCUIT

Fig.9

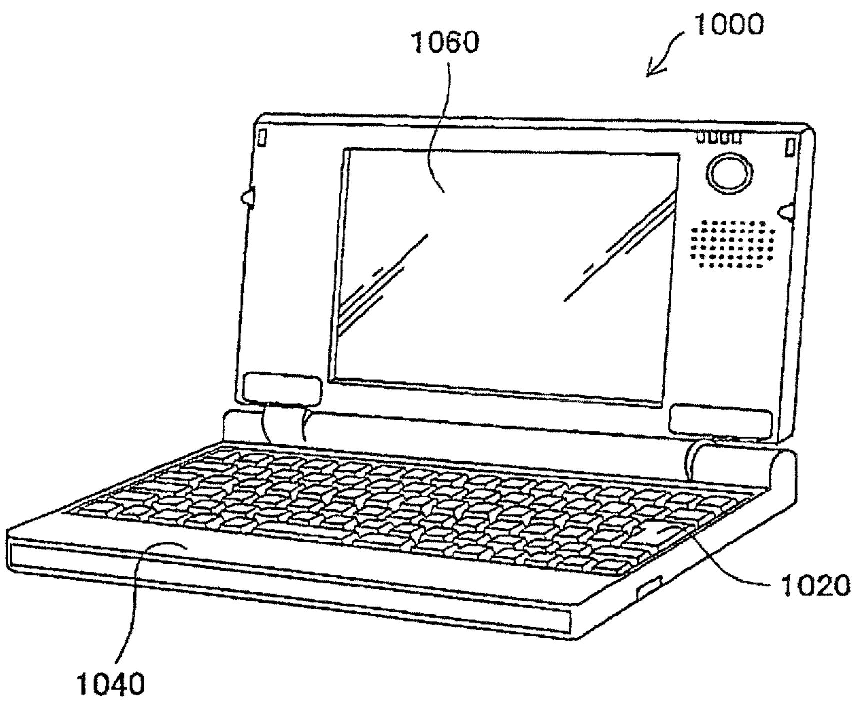


Fig.10

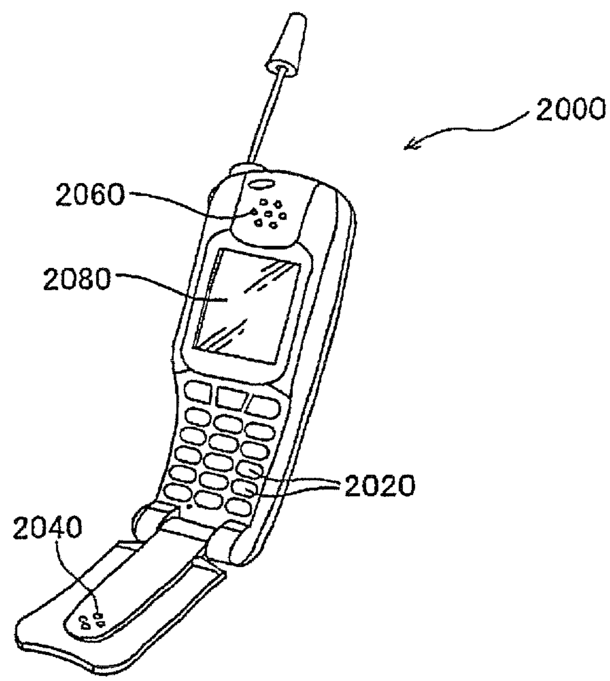
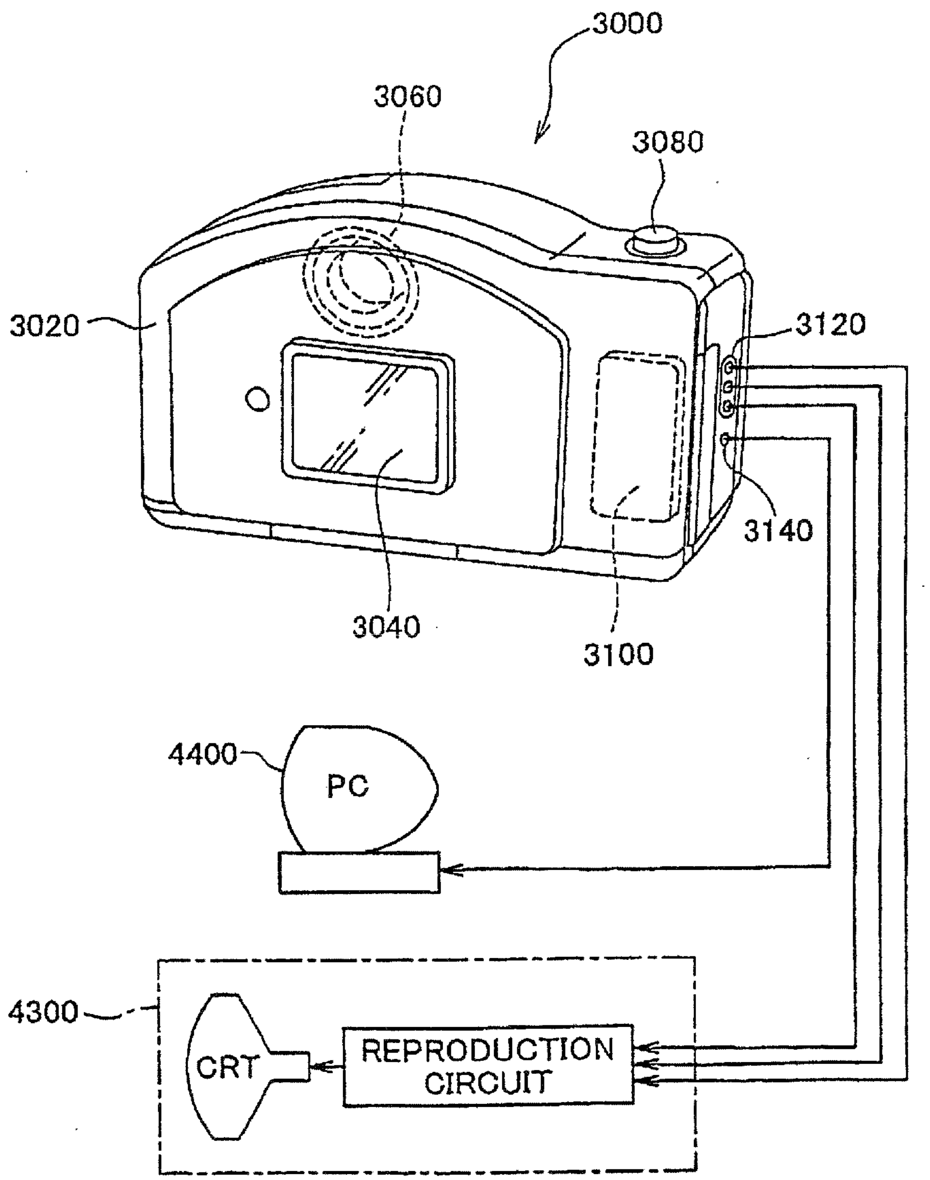


Fig. 11


3000
3060
3080
3020
3120
3140
3040
3100
4400
PC
4300
CRT
REPRODUCTION
CIRCUIT